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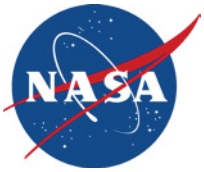

Reliability of CGA/LGA/HDI Package Board/Assembly

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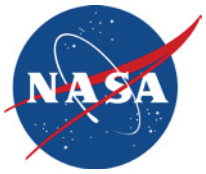

Reliability of CGA/LGA/HDI Package Board/Assembly

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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Objectives and Products

Commercial-off-the-shelf column grid array (COTS CGA) packaging technologies in high reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Understanding the process and quality assurance (QA) indicators for reliability are important for low-risk insertion of these advanced electronic packages.

This interim report presents test data for CGA packages with 1752 and 1272 inputs/outputs (I/Os) and 1-mm pitch. The CGA1752 package underwent visual, SEM, and thermal cycle evaluation and an assessment of the integrity of its chip capacitors. The two package types had different column styles. Both were assembled onto conventional printed circuit boards using standard eutectic tin-lead solder paste alloy. An inspection was performed to determine the quality of solder paste prints and measure solder paste volumes with three different alloy particle sizes. The inspection results are presented for representative of these solder paste prints. X-ray photomicrographs showing solder joint quality and workmanship defects of the assemblies illustrate these findings.

In addition, the evaluation included a ceramic array package with 1517 I/Os that built as a land grid array (LGA) with no column attachment. A number of LGAs were converted to CGAs by performing column attachment using two different column styles and sizes. For one column style, the integrity of column attachments were established by subjecting a number of columns to pull testing—first, as attached and, subsequently, at intervals during isothermal aging at 125°C. The pull test results are also presented.

The first part of the project included evaluation of assemblies with daisy packages and conventional printed circuit boards (PCBs). Subsequent evaluations are planned to include high density interconnect (HDI) PCB technologies for more effective density and accommodation of larger than 500 I/O package technologies. Ultimately, a system approach will be implemented based on lessons learned for effective reliability evaluation of assemblies with functional packages and HDI PCB technologies. The qualification guidelines, which are based on the test results for CGA/LGA/HDI packages and board assemblies, will facilitate NASA projects to use very dense and newly available FPGA area array packages with known reliably and mitigation risks, allowing greater processing power in a smaller board footprint and lower system weight.

Table of Contents

1. Executive Summary

The overall objectives and approaches of the reliability evaluation of CGA/LGA/HDI package/board/assembly are summarized in Figure 1 ─ topics marked with smiley faces will be presented in this interim report. The goal is to develop qualification guidelines for advanced high input/output (I/O) column/land grid array (CGA/LGA) assembled onto both conventional and high density interconnect (HDI) printed circuit/wiring boards (PCB/PWB). The report will address preliminary results for package evaluation and assembly optimization. Two CGA packages with 1752 and 1272 I/Os and two column styles were evaluated, one with a pure solder column and the other with a copper-wrapped solder column. Figure 2 shows photomicrographs of the packages and their column configurations.

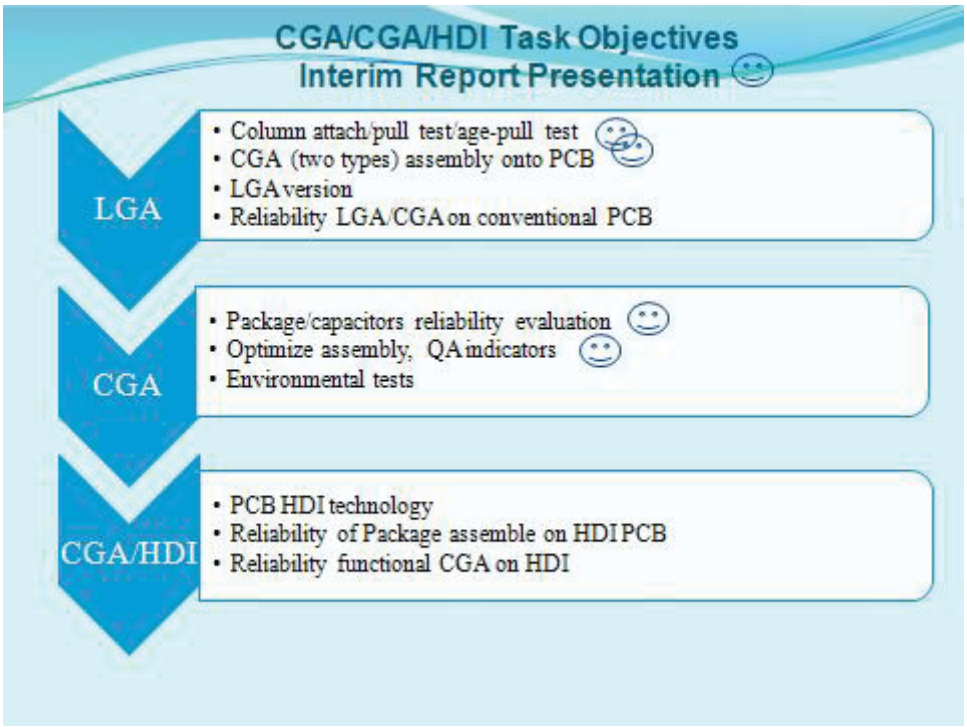


Figure 1. Test matrix for CGA/CCGA/HDI package/board/assembly program with identification of the areas covered in this report.

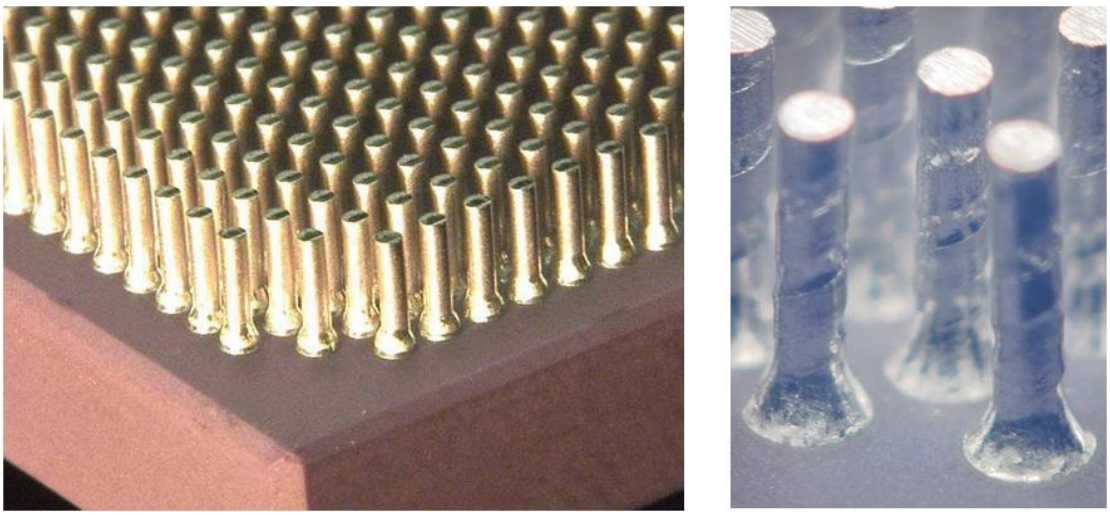


Figure 2. CCGA 1752 and 1272 I/O packages with pure solder column (left) and copper-wrapped solder column (right).

The scope of our evaluation also included a ceramic array package with 1517 I/Os that came as land grid array (LGA) with no column attachment. A number of these LGAs were converted into CGA by performing column attachment. Two facilities were used to perform column attachment, each having a unique column style. One style had copper wrapped onto a solder column with a diameter slightly lower than standard value; the other style had a micro-spring coil with no solder column, but a standard diameter. Photomicrographs of the LGA package and the two column types are shown in Figure 3.

The integrity of column attachment of the copper-wrapped column style LGAs was established by pull-testing; first, as attached and, subsequently, at intervals during isothermal aging at 125°C. After column attachment integrity was found to be acceptable, then column attachment was performed for the other LGA style. The pull test results to 500 hours of isothermal aging did show some sign of degradation due to solder column, but no changes in failure mechanism. All failures were due to column failures with no solder column interfacial failure, revealing that interface solder joint/attachment is stronger than column strength.

Visual, SEM, and thermal cycle evaluations were performed on the CGA1752 package to determine the integrity of the chip capacitors, which were previously surface-mounted onto the ceramic substrate of the package. No failures of the high-lead chip capacitor solder joints were observed when packages were subjected to 200 thermal shock cycling in the range of –55°to 130°C, with 10 minutes dwell times, at the two extreme temperatures.

The 1752 and the 1272 I/O packages with two different column styles (pure solder and copper-wrapped columns) were assembled onto conventional printed circuit boards using standard tin-lead solder paste alloys. The inspection results of the peripheral columns after assembly revealed that the quality of solder joints was acceptable. X-ray photomicrographs, showing the quality of solder joint assemblies and applicable workmanship defects, revealed no shorts or significant solder balling.

In summary, it was demonstrated that LGA could be successfully converted into CGA packages using either of the two column styles. Furthermore, these types of CGA packages could be successfully assembled onto conventional PCBs if the PCB pad design and other

processing parameters were appropriately optimized for the column styles and package sizes. Extremely large/thick CGA packages with 1752 I/Os were successfully assembled onto PCBs. Reliability is a key issue that was addressed for chip capacitors on packages, but the overall board level assembly reliability is slated for evaluation and inclusion in the final report, for both conventional and HDI PCBs.

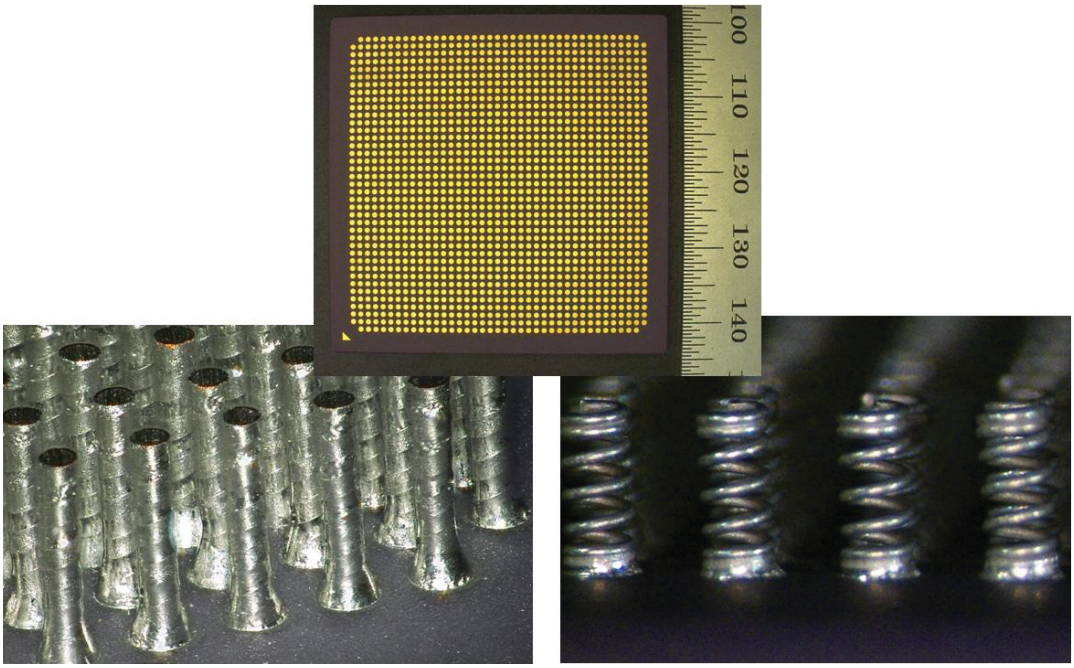


Figure 3. Land grid array (LGA) before column attachment (top) and after both copper-wrapped solder column attachment (left) and microspring attachment (right).

2. CGAs and Evaluation Approaches

2.1 Column Grid Array Packaging Technology Trend

For high reliability applications, lower I/O CGAs with a 1.27-mm pitch (the distance between adjacent column centers) are replacing surface-mount leaded packages, such as ceramic quad flat packs (CQFPs). There are no comparable ceramic leaded packages for higher I/O CGAs. The advanced CGA packages, those with more than 1000 I/Os, generally come in 1-mm pitch and use flip-chip die rather than wire bond internal to the package. Replacement to CGA is especially appropriate for packages with higher than 300 I/O counts where CQFP pitches become much finer (0.3-0.4 mm), making them extremely difficult to handle and assemble. In addition to size reduction, CGAs also provide improved electrical and thermal performance and are the package choice for field programmable gate arrays (FPGAs). However; their solder columns are prone to damage, it is challenging to assemble them onto PCB, and it is almost impossible to rework defective solder joints.

Rework, re-attachment of columns, and reassembly prior to final assembly may be required to address solder defects due to processing or column damage due to shipping and mishandling. The CGA packages are in the form of LGA during initial die attachment and underfilling; later columns are attached under another processing step. This report will address several pertinent issues: the integrity of LGAs after column attachment process; the integrity of CGA packages with chip capacitors; and the solder joint reliability of both LGAs and CGAs after they are assembled onto PCBs.

CGA packages are preferred to CBGA (see Figure 4) since they show better thermal solder joint reliability than their CBGA counterparts. For most high reliability applications, CGAs show acceptable solder joint reliability for larger packages and higher than 300 I/Os (when resistance to thermal cycling is significantly reduced for CBGAs with increasing package size and I/Os). To limit the growth of package size, most ceramic packages with more than about 1,000 I/Os come in the CGA style with 1-mm pitch or lower.

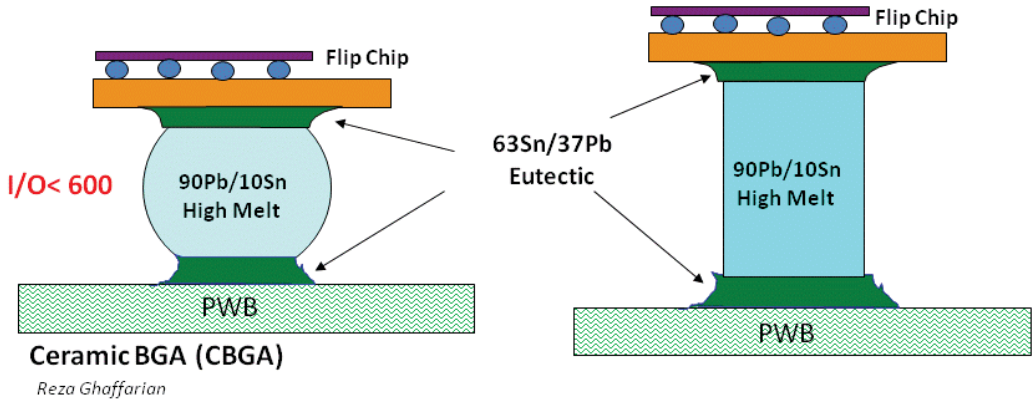


Figure 4. Examples of ceramic column grid array (CCGA or CGA) and ceramic ball grid array (CBGA) package configurations.

The key drawback of CGAs remains the same: individual column re-workability is impossible and inspection capability for interconnection integrity is poor (e.g., cannot detect cracks or cold solder). Implementation of process controls is critical in achieving quality solder joints, which consequently achieves optimum assembly reliability. Visual inspection of peripheral columns, when they are not blocked, is possible to be performed by optical microscopy to ensure solder quality as another process indicator. Although progress has been made in improving the resolution of X-ray for better inspection, the issue of inspection for specific defects, such as cold solder joints and microcracks, remains unresolved.

Even though CGAs are commercial-off-the-shelf (COTS) packages, their high reliability versions go through a much more stringent screening, which adds significant cost and longer delivery times. The issues with CGA COTS packages are essentially the same as other COTS issues and include package die source and lot-to-lot materials variations, availability of packages with radiation-hard die, outgassing for materials including underfill, etc. A number of these issues are addressed for high reliability versions. Assembly, inspection, and lack of individual solder reworkability issues are additional key aspects of such implementation. Assembly reliability behaviors of such area array packages, including CGAs, are addressed in a number of previous investigations [1]–[6].

2.2 Purpose of This Interim Report

This interim report presents test data for CGA packages with 1752 and 1272 I/Os and 1-mm pitch. It includes the results of visual, SEM, and thermal cycle evaluations performed on the CGA1752 packages to determine the integrity of the chip capacitors on package. After integrity was established, packages were assembled onto conventional printed circuit boards using standard tin-lead solder paste alloys. Inspection was performed to determine both the quality of solder paste prints and the volume of three solder paste types with different solder particulate sizes. Results are also presented for inspections performed on two packages with different dimensions and column types. X-ray photomicrographs show the quality of solder joint assembly and workmanship defects.

Evaluation also included a ceramic array package with 1517 I/Os that was originally an LGA. A number of LGAs were transformed into CGA by performing column attachment using two different column styles. The integrity of column attachment for these was established by subjecting them to pull testing; first, as attached and, subsequently, at intervals during isothermal aging at 125°C. The pull test results are shown.

3. Experimental Approaches for CGA Packages

3.1 CCGA Package Types

The evaluations covered in this report deal with several aspects of advanced area array packaging and high density printed circuit boards. One was to characterize the reliability of CGA packages with 1752 and 1272 I/Os and 1-mm pitch, assembled onto conventional PCBs. Figure 5 shows photomicrographs of the two CGAs and their sizes. These daisy chain CGA packages were built by two different manufacturers and had two different column styles. The cost of the larger daisy chain package was five times more than the smaller one. Since CGA daisy chain packages are typically 50 to 300 times more expensive than PBGA daisy chain versions, only a very limited number were used. This section presents preliminary test results for packages and assembly optimization.

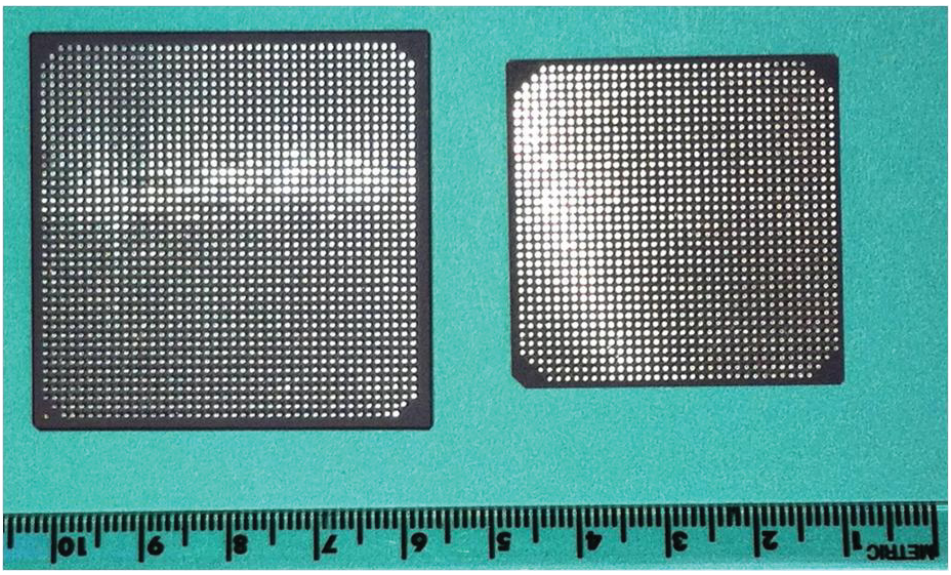


Figure 5. The two column grid array (CGA) packages; 1752 I/Os (left) and 1272 I/Os (right). Note that in both cases corner columns are removed by the manufacturer.

3.2 CCGA Package Receiving, Inspection, and Evaluation

The two CGA package types were inspected by microscope to detect any workmanship defect anomalies, such as bent columns, and to verify the quality and uniformity of solder joints for column attachments (see Figure 6, for representative photomicrographs of the two packages.) The 1752 package has pure tin-lead solid solder with high lead concentration (90Pb/10Sn); the 1272 CGA package has slightly lower lead solder content (80Pb/20Sn), but solder columns are wrapped with copper helical spring. Copper-wrapped columns are also tin-lead coated and therefore do not have the appearance of copper except for the exposed flat area on top.

The CGA1272 is hermitically sealed with no additional chip capacitor parts. The CGA1752 is non-hermetic, has an additional chip capacitor on top of the ceramic substrate,

and is exposed. Figure 6 shows a generic construction of this package provided by the manufacturer along with a photo of the package from the top. Inspection of chip capacitor solder joints for a package received in December 2010 revealed a number of unacceptable solder joints, based on NASA workmanship standards. For this reason, the solder joints for these chip capacitors were further characterized by SEM and subjected to a limited number of thermal shock cycles. The results of inspection and environmental evaluation are discussed in the following sections.

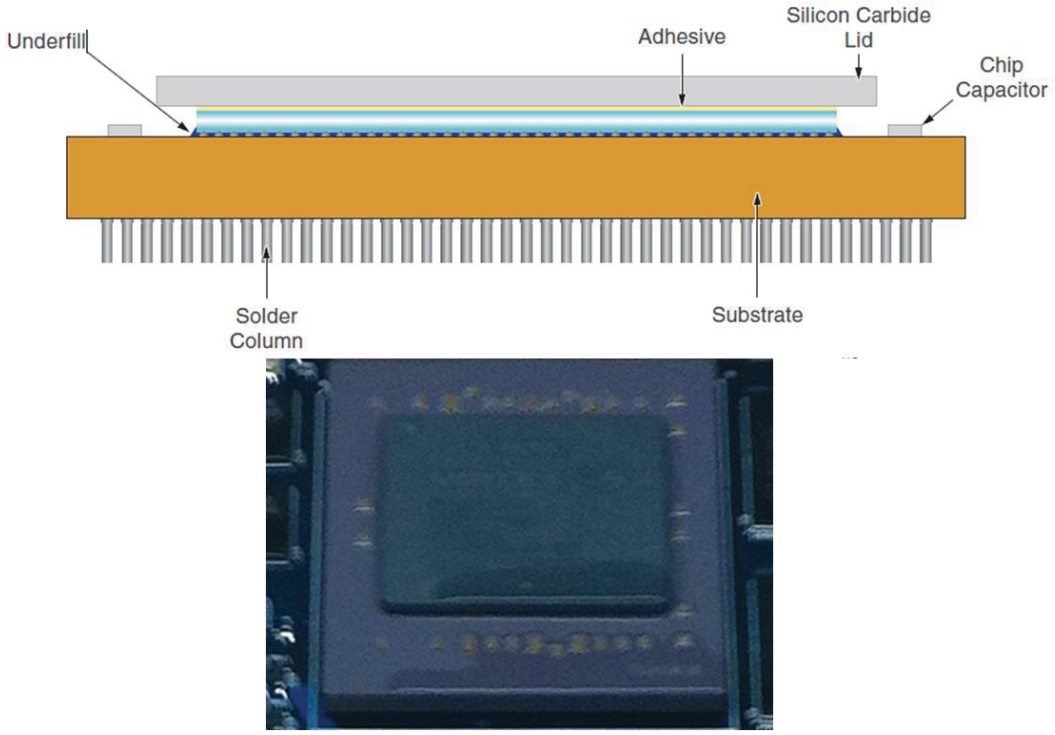


Figure 6. Construction of CGA 1752 I/O package (top) and photo of package showing the exposed chip capacitors.

3.2.1 CGA Package Characterization by X-ray

A real-time 2D X-ray system was used to determine the integrity of column solder joint attachment, among other features of these packages. Figure 7 shows representative X-ray photomicrographs of CGA1752 and CGA1272.

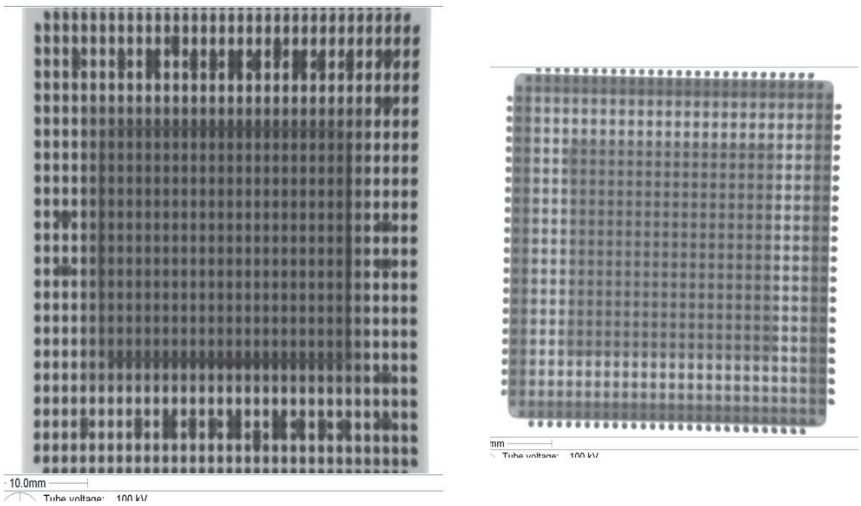


Figure 7. X-ray photomicrographs of CGA 1752 I/Os (left) and CGA 1272 I/Os (right); the darker areas are where chip capacitors are located.

3.2.2 Chip Capacitor Characterization

The first set of daisy chain package samples was received late in December of 2010. Inspections revealed workmanship deficiencies of chip capacitor solder joints, which are formed into the side metallization rather than conventional two-end solder joints. Figure 8 shows optical photomicrographs of representative solder joints. There are six (6) 0805 and twenty-five (25) 0603 capacitors, making a total of 248 solder joints. Thorough inspection of one package revealed that out of 248 solder joints, 24 showed potentially poor quality, based on NASA workmanship requirements.

An extreme case of shifting away from side metallization on a package with unacceptable solder joints is shown in the following figure (the far right joint). Note that these are daisy chain packages and may not be representative of a functional package. Functional packages should be inspected for such workmanship anomalies before committing to an expensive assembly process and extremely difficult rework process.

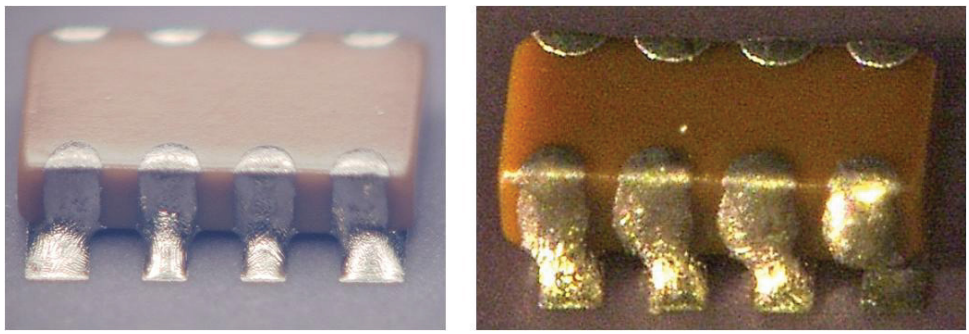


Figure 8. Chip capacitors showing inconsistency in solder joint quality; the far right solder is clearly unacceptable.

Further characterizations were performed using scanning electron microscopy (SEM) to better define microstructure. Figure 9 shows a representative example of solder joint quality at a higher magnification.

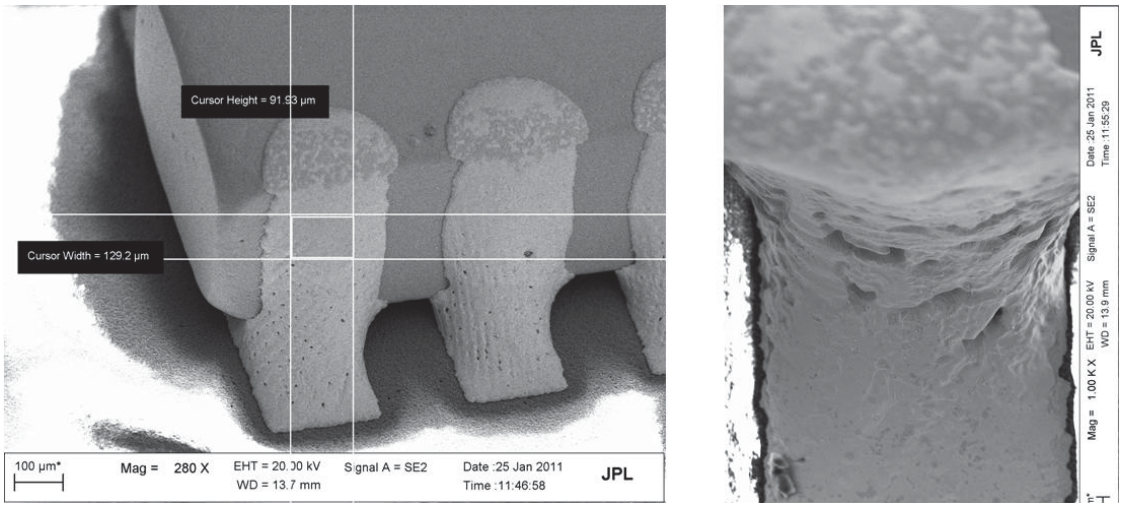


Figure 9. SEM photomicrographs showing the nature of solder joints at much higher magnification.

In addition, elemental analysis was performed using dispersive X-ray spectroscopy (EDX/EDS) to obtain semi-quantitative elemental results for the solder joints. The results showed that indeed they are high lead tin-lead solder (see Figure 10), similar to the column solder alloy. The melting point of these solder alloys is higher than the tin-lead commonly used to attach columns onto PCB. High lead solders generally show a lack of shininess and poor flow. This is due to their alloy pasty regime during solidification when they are compared to eutectic tin-lead solder, with no pasty regime during melting.

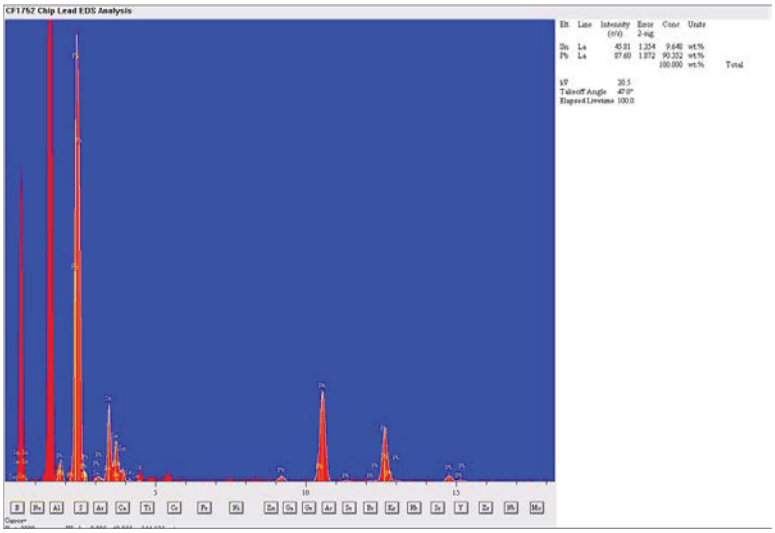


Figure 10. EDX/EDS elemental analysis showing that solder alloy has high lead (90/10).

3.2.3 Chip Capacitor Characterization After Thermal Shock Cycles

CGA1752 and CGA1272 packages with different column styles were subjected to thermal shock cycles to specifically establish resistance of chip capacitor solder joints (for CGA1752) and to inspect the integrity of solder column attachments. To establish behavior of high lead solder joints under thermal cycling and subsequent reflow during assembly, the thoroughly inspected package was subjected to thermal shock cycles. This was accomplished by using two chamber cells and cycling between –55° to 130°C, with 10 minutes dwell times at the two extreme temperatures. Samples were removed after 50 cycle intervals and inspected for signs of damage and degradation due to thermal shock cycles.

Figure 11 shows representative solder joints after 200 thermal shock cycles. No evidence of significant damage or crack initiation was observed. Resistance of solder joint to thermal shock is attributed to good CTE match of ceramic chip capacitors to ceramic CGA substrate. The higher melting temperature of high lead tin-lead solder also contributed to its high resistance to thermal shock cycle.

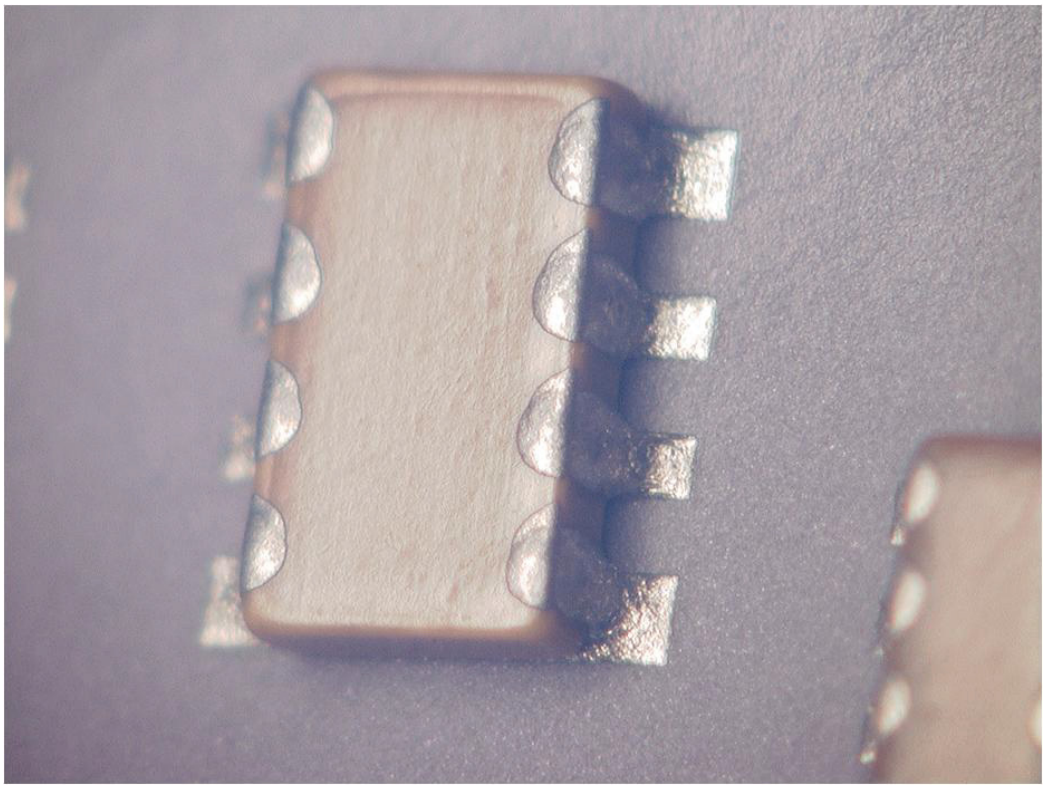


Figure 11. Chip-capacitor solder joint quality after 200 thermal shocks (–55° to 130°C) showing no signs of cracks.

3.2.4 Chip Capacitor Characterization—Newer Samples

The second set of daisy chain package samples was received late in May 2011. Inspection revealed much lower workmanship deficiency of the solder joints for chip capacitors, compared to those received the previous December. Figure 12 is an optical photomicrograph

representative of the side solder joints. For this new batch only 7 out 248 solder joints were marginally acceptable, using the NASA workmanship standard as a baseline. This is a significant improvement compared to the previous batch, indicating a more stringent quality control. Nonetheless, an inspection plan may be required to be implemented at receiving to assure adequate quality of solder joints.

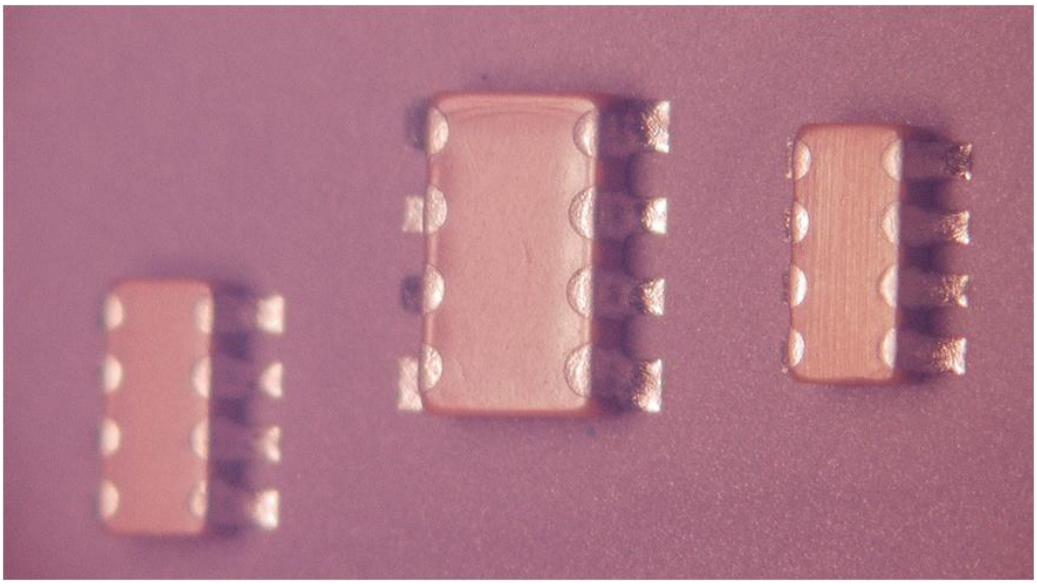


Figure 12. Chip capacitors showing better solder joint quality in the May 2011 set.

3.3 Test Vehicle Design and Assembly Parameters

To determine assembly reliability of the two CGA daisy chain packages, the board was designed to match CGA patterns. Not all packages styles from a manufacturer come in daisy chain form; generally, manufacturers only select representative packages and offer them as daisy chain, so the choice of packages for evaluation is limited. The daisy chain patterns on PCB were designed to complement CGA patterns, forming a complete loop after assembly. The resistive loop is generally monitored during thermal cycling to allow detection of open loops due to solder joint opens of CGAs onto PCB. The two daisy chain CGA packages, even though built by two different manufacturers, had roughly the same column dimensions.

A complex PCB was designed to accommodate the two CCGA packages and also to provide sites for other advanced fine-pitch array and leaded/no-lead packages. Figure 13 shows the board design, with daisy chain pattern, and how traces are routed to the edge of the board for daisy chain monitoring.

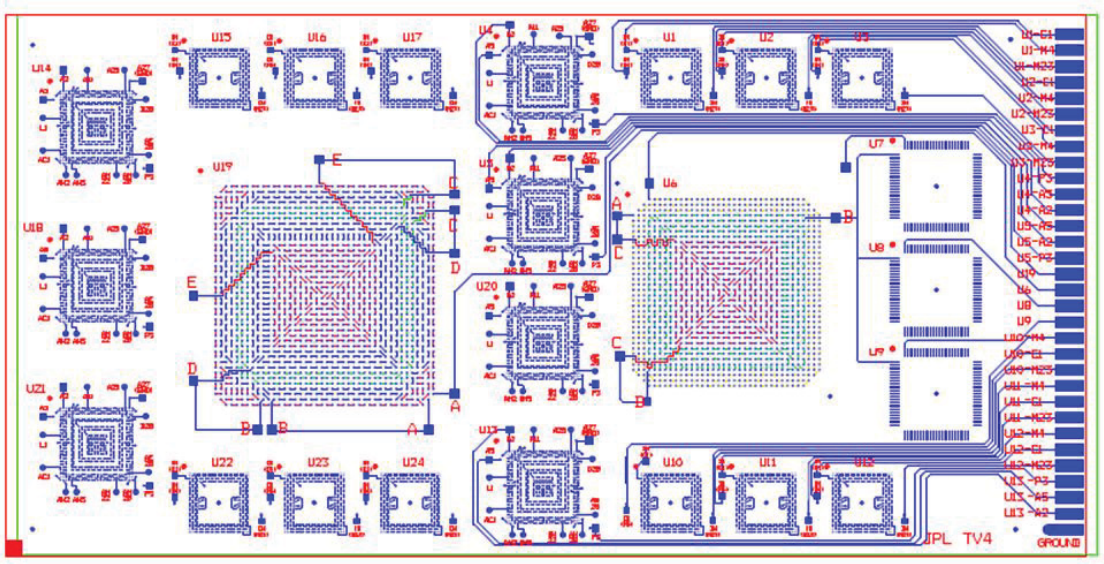


Figure 13. Test vehicle design showing both combined package and board daisy chain patterns for the two CGA packages. A few other daisy chain patterns currently not used for evaluation are also apparent in the design.

A design of experiments (DOE) technique was used to cover various aspects of processing and packaging assembly reliability. The following packages and parameters were evaluated as part of a larger DOE implementation:

- The CGA1752, with 1.0-mm pitch and 42.5-mm^2 body size, designed with enough space for rework evaluation at one side. Numerous daisy chains were designed on board to compliment daisy chains on a package, in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- The CGA1272, with 1.0-mm pitch and 37.5-mm^2 body size, designed with enough space for rework evaluation. Lead parts are designed to determine the influence of rework visually. Numerous daisy chains were designed on board to compliment daisy chains on a package, in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- Boards were made from high glass transition temperature (Tg) FR-4 materials with 0.093-inch thickness. They had a hot air solder leveling (HASL) tin-lead surface finish commonly used for tin-lead solder.
- A standard 6-mil-thick stencil was used for paste printing of the whole board when only the two CGAs are to be built. However, other stencil thicknesses or use of a mini stencil may be required to accommodate building a board of this complexity, or if reworking is performed.
- Three types of solder paste were evaluated for paste print quality. Solder paste volumes were measured at the four corners and at the center for several assemblies to document actual paste print volume, distribution, and solder paste release efficiency.

- Vapor phase reflow was used to assemble the two CGA packages. Placement of CGAs, however, was done using a rework station.

These assemblies were first subjected to inspection and daisy-chain continuity checks to determine manufacturing robustness of various package configurations. Figure 14 shows an assembled test vehicle. They will be then exposed to a number of environmental conditions to evaluate their reliability and failure mechanisms. Both the paste print quality evaluation and also inspection after assemblies are discussed below.

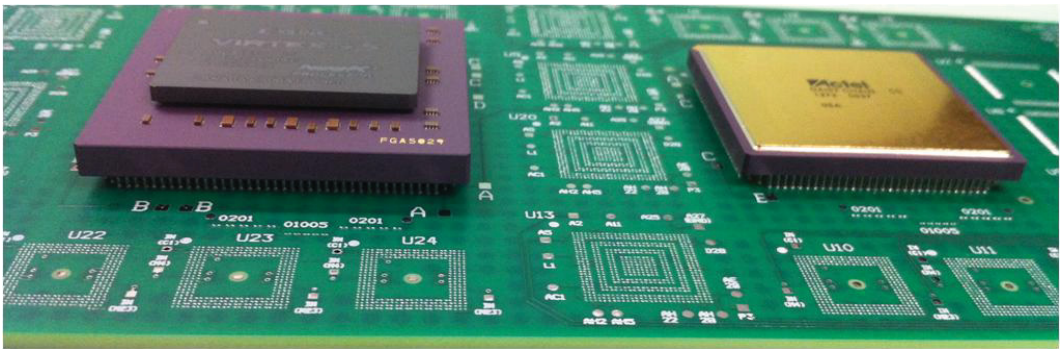


Figure 14. Assembled test vehicle showing the two CGA packages with different sizes and column styles.

3.4 Solder Paste Volume Measurement

Achieving a proper stencil design that accommodates both CGAs and other advanced packages is challenging. There are many variables to be considered, including stencil thickness, aperture opening, and solder paste type. The paste type is considered to be the most critical factor for finer pitch package assembly, but may have minimum effect on the assembly quality of CGA packages. Three types of solder pastes were considered:

- Type III (−325/+500, mesh size) RMA pastes, solder particle diameter between 20 and 45 microns, commonly used for conventional packages. Paste deposition on the PCB pad's patterns was accomplished using a paste print machine with standard parameters, including paste print speed and 1:1 aperture opening.
- Type IV (−400/+625, mesh size) RMA paste with slightly higher cost and solder particle diameter (between 20 and 38 microns) was used to improve assembly yield for conventional and potential fine pitch array packages.
- Type V (−500, mesh size) RMA paste, with even finer particle diameter (between 10 and 25 microns)..

The rule of thumb for an aperture opening size is to be about four to five times the solder powder diameter. After deposition, each paste print was visually inspected using a microscope for detecting gross defects, such as bridging or insufficient paste deposition. On extremely rare occasions, print quality was improved by either adding a small amount of solder paste when insufficient paste was detected or by removing solder paste from the

connecting pads when bridging was discovered. Figures 15 shows representative photomicrographs of paste print and quality for the CGA1272 and CGA1752 I/O packages. Note the daisy chain pattern on board that compliments the packages.

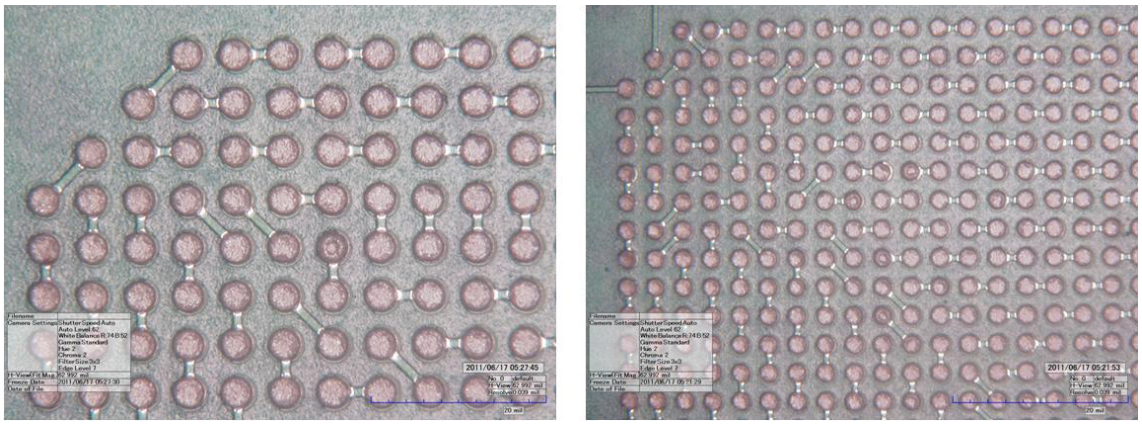


Figure 15. Representative photomicrographs of paste print deposition quality for the CGA1272 I/O (left) and CGA1752 I/O (right).

In addition, solder paste areas and heights were measured using a laser interferometer profilometer with a sophisticated three-dimensional (3D) measurement capability. Measurements were taken at numerous locations—including corner and center pads—to gather solder volume data and their corresponding distributions.

Figures 16 to 18 show photomicrographs of CGA1752 pads after solder paste deposition and their characteristic parameters, including height values for type III–V pastes. The figures also show color-coded height distribution of solder paste prints for these sets of pads. Overall, no major manufacturing issues were encountered with the paste depositions for the two CGAs with 1.0-mm pitches. In general, there were no significant differences among the three solder paste types for the CGAs, even though a sharper height periphery was observed as the size of solder paste particulates decreased from type III to type V.

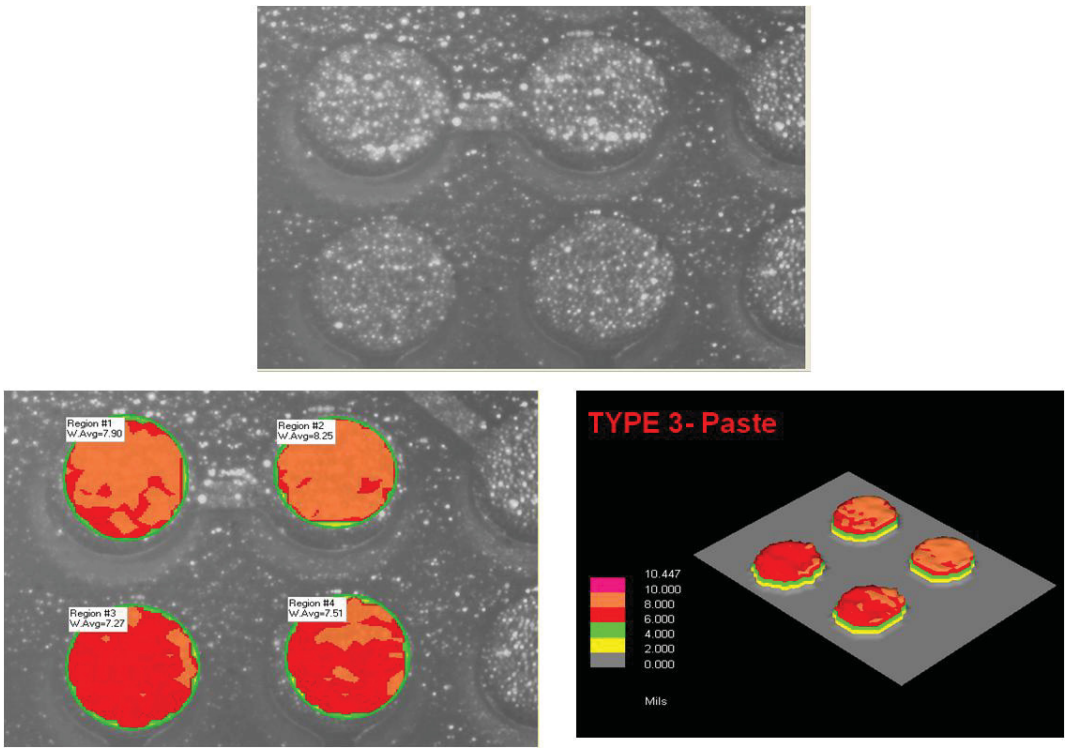


Figure 16. Type 3 solder paste print quality and color-coded height distribution for CGA1752 I/O.

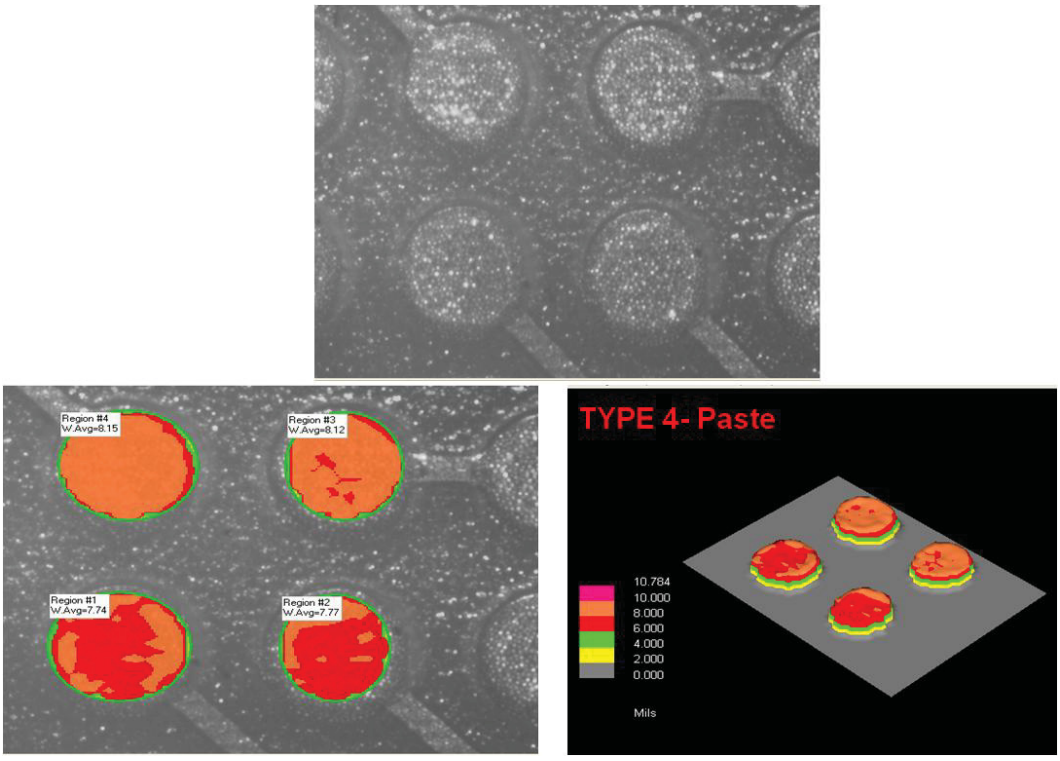


Figure 17. Type 4 solder paste print quality and color-coded height distribution for CGA1752 I/O.

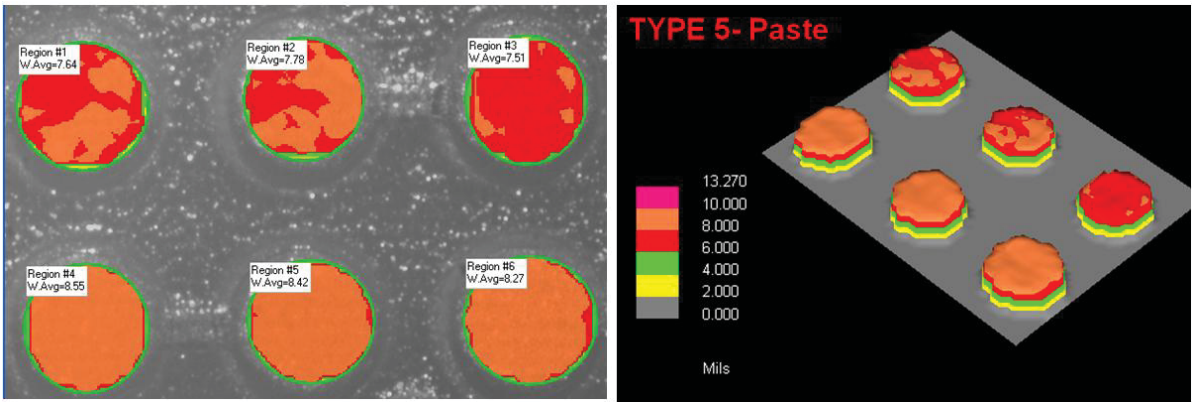


Figure 18. Type 5 solder paste print quality and color-coded height distribution for CGA1752 I/O.

Figure 19 shows plots of solder height distribution for three different paste types using a 6-mil stencil thickness with a 28-aperture opening. The height measurement was relative to a few surface areas at each location, not relative to copper traces; therefore results shown are a copper thickness higher that actual height values. Different solder paste types showed similar trends and heights, considering the potential of other paste print variations. Nevertheless, the height did not correlate with the solder paste particulate sizes; it did not increase as particle sizes decreases. It increases first from paste type III to type IV and then decreases for type V, fitting values between the two.

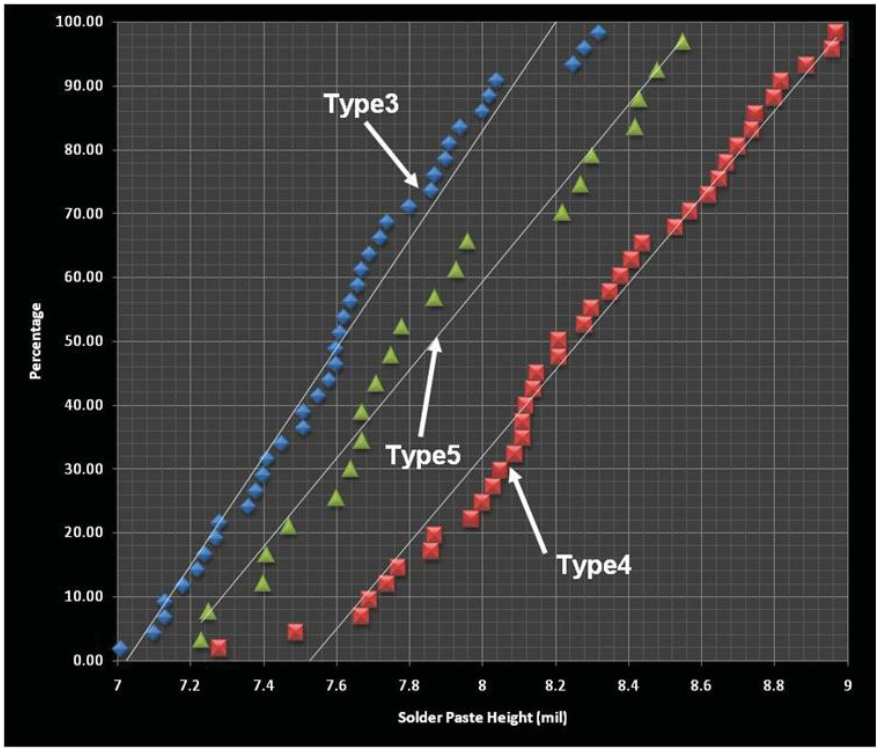


Figure 19. Comparison of paste print height distribution of CGA1752 and 1272 I/O pads for type 3, type 4 and type 5.

3.5 Attachment Procedures

Intentionally, a large number of fine pitch array advanced packages and leaded quad flat packages were designed close to the CGA packages. The reason for this configuration was to determine paste print quality and manufacturing challenges associated with a large column grid array package surrounded by small, fine pitch ones. Initial activity only concentrated on assembling large CGA packages, since these packages are new, with no heritage experience on assembly. Package placement was accomplished using a rework station.

Solder paste reflow was performed using a vapor phase reflow machine set up for the tin-lead process. Reflow profiles were based on a previously established profile that was tailored using a sample run with the attached thermocouple generating the reflow thermal profile. Vapor phase consists of an infrared preheating followed by a constant temperature boiling vapor zone. Infrared preheating temperature and time, as well as time in vapor phase, are the only key parameters that can be modified to achieve better solder attachment quality.

4. Test Results After TV Build

4.1 Daisy Chain Resistance Results

To verify assembly process acceptance, daisy chain resistances for CGA package assemblies were verified after the first test vehicle (TV) build and found to be continous and acceptable. The measurements were also taken for subsequent TVs after their built. Specifically, this provided the baseline to compare against any differences in resistivity for the type III–V solder pastes evaluated in this investigation. All packages had a pair of connected pads, which complemented specific pairs of PCB pads to build loops of continuous daisy chains for solder joint opens. There are 5 daisy chain patterns for CGA1752 and 3 patterns for CGA 1272. A short could be detected when lower-than-nominal resistance values were measured. Except for relatively low solder balls, no shorts were observed for CGAs by X-ray. The results of manufacturing yield and daisy chain resistances for various conditions of assembly using vapor reflow are summarized in Table 1. Manufacturing yield for CGAs was favorable, with no opens for those assembled.

Table 1. Summary of daisy chain resistance measurements (in Ohms) within each CGA package, after assembly, using paste types III–V.

ID	Paste Type & Process	A-1752	B-1752	C-1752	D-1752	E-1752	A-1272	B-1272	C-1272
TV5-001	Type5 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	0.76	10.71	10.61	11.50	12.02	1.92	2.53	2.15
TV5-002	Type3 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1273	7.18	10.10	9.97	10.79	11.26	1.88	2.46	2.07
TV5-003	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1274	7.61	10.74	10.63	11.48	12.01	1.88	2.50	2.11

4.2 Inspection

For high-reliability electronic applications, visual inspection is commonly performed by quality assurance (QA) personnel at various levels of packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria established for high-reliability applications. Further assurance is gained by subsequent short-time environmental exposure, including thermal storage, thermal cycling, vibration, mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space applications, generally 100% visual inspection is performed for the hybrid package, both pre-sealing (pre-cap) and after assembly prior to shipment. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level.

For CGA package assembly, visual inspection of peripheral columns with solder joints is possible if they are not blocked. Such inspection provides valuable information on solder joint attachment and process quality. It is impossible, however, to inspect hidden columns under the package. X-ray evaluation is needed to determine shorts and, on rare occasions, opens, for area array packages. For the test vehicle with daisy chain package configuration, verifications were performed using:

(1) Daisy chain continuity checking

(2) X-ray quality detection for shorts, and on rare occasions, for opens

(3) Visual inspection with optical microscopy photographs of peripheral columns

For the CGA assemblies, except for solder balls, no shorts were detected by X-ray and no opens, which sometimes are apparent by being a smaller, darker area. In addition, no apparent cracks or other anomalies were seen with an optical microscope. Extensive X-ray and optical characterization was performed, but only a few representative photomicrographs documenting quality were shown.

4.3 X-Ray Characterization

X-ray inspection was performed, following visual inspection and the daisy-chain continuity check, to selectively verify package/assembly conditions. The 2D real time X-ray transmission system with oblique angle views was utilized for this inspection. Figure 20 shows representative X-ray photomicrographs for the CGA1752 and CGA1272 packages after assembly, marking a potential open with an arrow.

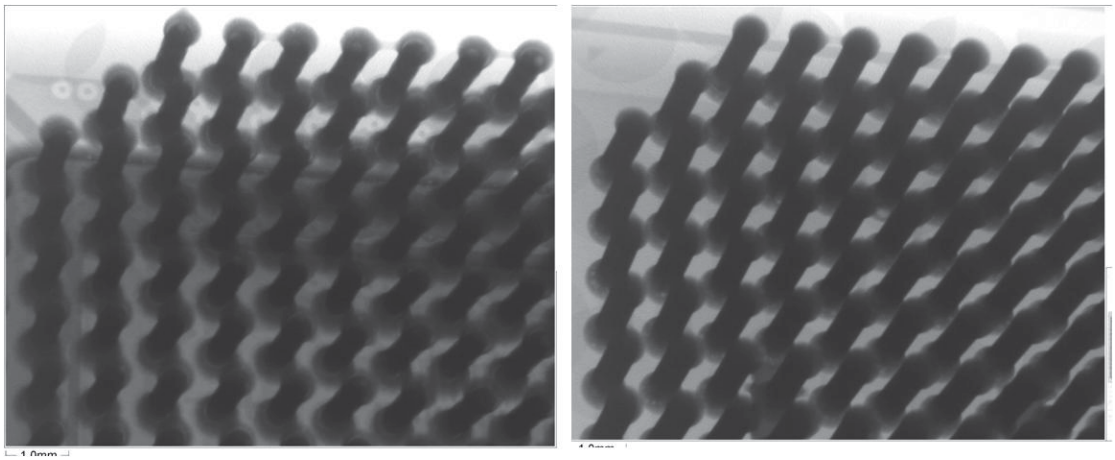


Figure 20. As-assembled X-ray photomicrographs for the CGA1272 I/O (left) and CGA1752 I/O (right). There were no signs of shorts.

4.4 Optical Microscopy Characterization

Visual inspection of peripheral columns was performed for most assemblies, since the board was designed for visual characterization (most of the PCBs were only populated with CGAs). Only outer row, and in some cases, second and third rows could be assessed for solder joint quality. The representative photomicrographs in Figure 21 show the quality of solder joints for CGA1752 and CGA1272 I/O assemblies. Note that solder joint fillet formations are different for the pure column and copper-wrapped solder columns. Solder joints were generally acceptable even though they appear different wetting and column peripheral cover ages.

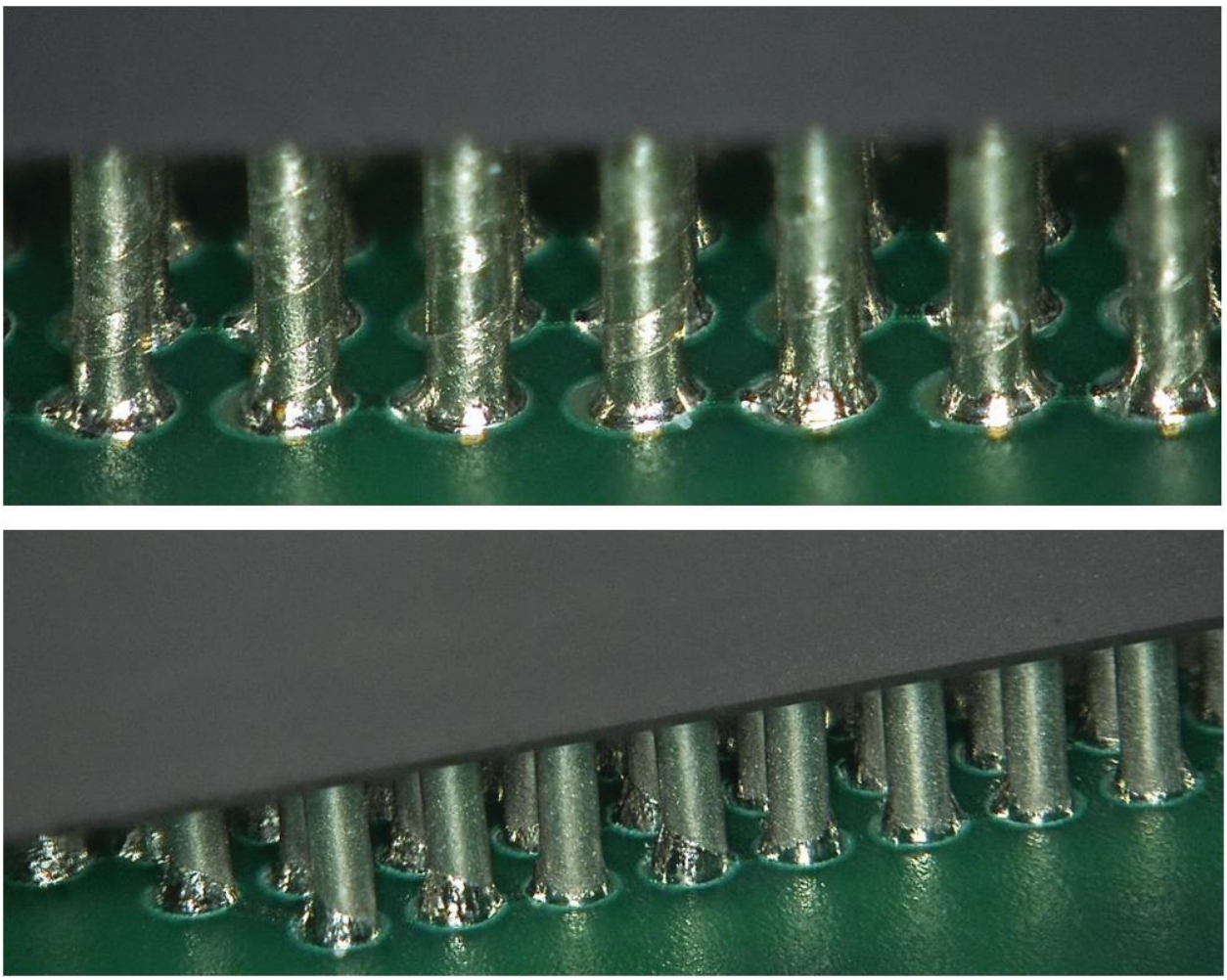


Figure 21. Representative photomicrographs of solder joint quality after assembly for CGA1272 (top) and CGA1752 (bottom).

5. Experimental Approaches for LGA Packages

5.1 LGA Column Attach

This report covered many aspects of advanced area array packaging and high density printed circuit boards. The purpose of the following aspect of the investigation was to characterize the reliability of LGA1517 packages with 1-mm pitch. LGAs were subject to both copper-wrapped column and micro-spring coil attachment for subsequent evaluation. Column attachment integrity was evaluated by subjecting a CGA version to isothermal aging and pull tested before and at intervals during environmental aging. Figure 22 shows photomicrographs of the LGA package after it was transformed to CGA.

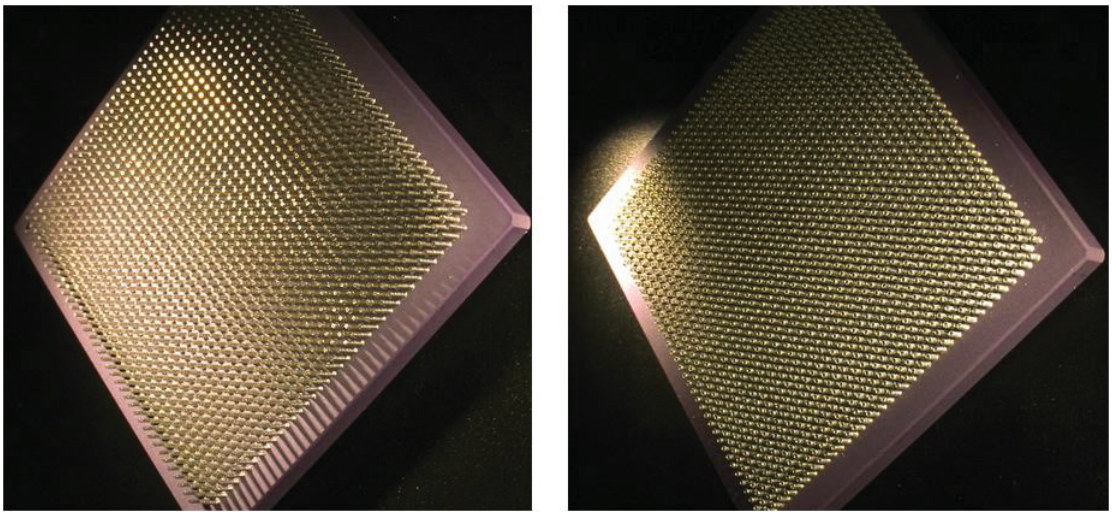
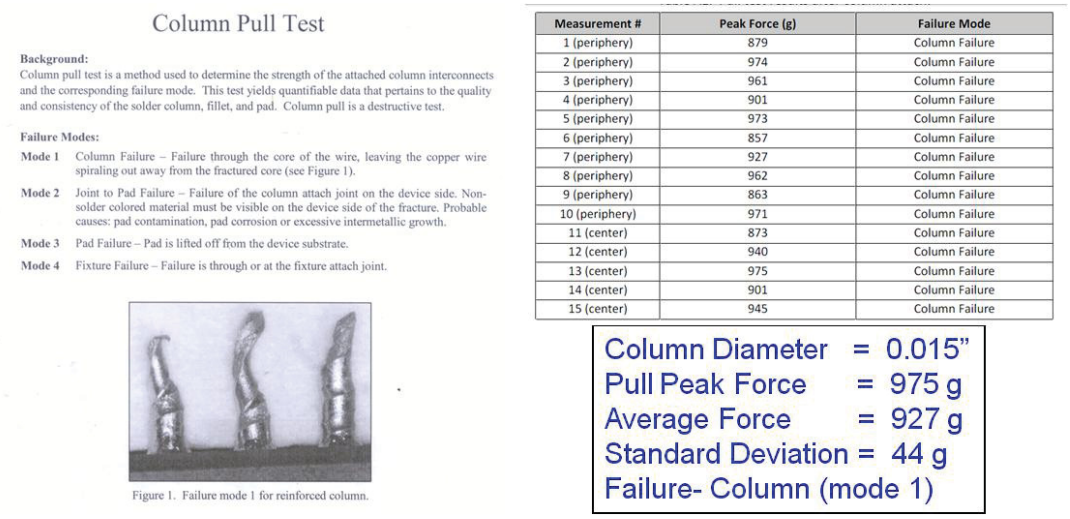


Figure 22. Representative photomicrographs of an LGA package after copper column (left)and micro-spring coil column (right) attachment.

5.2 Pull Strength of Column Attachment: Pre- and Post-Aging

Initially, one LGA was subjected to column attachment and integrity verification prior to the full commitment of other LGA packages. LGA columned packages were subjected to pull testing to determine the strength of copper spiral columns and attachment integrity at interfaces. A small solid cylinder with a diameter of a few columns was attached to a column (~15 mils) for pull testing. Load values and failure modes were recorded. Figure 23 summarizes values for a number of columns that were pull tested. It also includes failure modes; all had ductile failure of the columns with no failures at the attachment interconnections. The average force applied was 927 g, with standard deviation of 44 g, a very consistent column quality and good metallurgical bonding result with no observed interfacial failure.



Column Pull Test

Background:
Column pull test is a method used to determine the strength of the attached column interconnects and the corresponding failure mode. This test yields quantifiable data that pertains to the quality and consistency of the solder column, fillet, and pad. Column pull is a destructive test.

Failure Modes:

Mode 1 Column Failure – Failure through the core of the wire, leaving the copper wire spiraling out away from the fractured core (see Figure 1).

Mode 2 Joint to Pad Failure – Failure of the column attach joint on the device side. Non-solder colored material must be visible on the device side of the fracture. Probable causes: pad contamination, pad corrosion or excessive intermetallic growth.

Mode 3 Pad Failure – Pad is lifted off from the device substrate.

Mode 4 Fixture Failure – Failure is through or at the fixture attach joint.

Figure 1. Failure mode 1 for reinforced column.

Measurement #	Peak Force (g)	Failure Mode
1 (periphery)	879	Column Failure
2 (periphery)	974	Column Failure
3 (periphery)	961	Column Failure
4 (periphery)	901	Column Failure
5 (periphery)	973	Column Failure
6 (periphery)	857	Column Failure
7 (periphery)	927	Column Failure
8 (periphery)	962	Column Failure
9 (periphery)	863	Column Failure
10 (periphery)	971	Column Failure
11 (center)	873	Column Failure
12 (center)	940	Column Failure
13 (center)	975	Column Failure
14 (center)	901	Column Failure
15 (center)	945	Column Failure

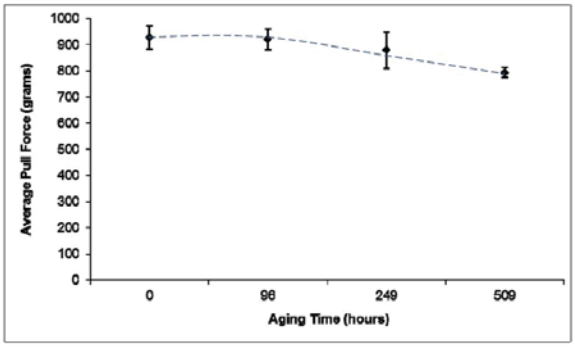
Column Diameter = 0.015”
Pull Peak Force = 975 g
Average Force = 927 g
Standard Deviation = 44 g
Failure- Column (mode 1)

Figure 23. Summary information of a representative column’s pull-test results.

One key concern is interconnection degradation due to high temperature exposure during assembly and application. To address this concern, the LGA package with columns was exposed to isothermal aging at 125°C for a total of 500 hours. Pull testing was performed at 96, 249, and 509 hours of aging to determine degradation with time.

The average pull-strength variations with time are shown in Figure 24. Pull strength values decreased slowly initially and then showed further decrease with time, for a total decrease of 14% at 509 hours. Student t-test calculations (paired two samples for means), at a confidence level of 95%, show that:

- There is no statistical difference between no aging and 96 hours of aging
- There is a statistical difference between 96 hours and 249 hours of aging
- There is a statistical difference between 249 hours and 509 hours of aging



Aging Time (hours)	Average Pull Force (grams)	Standard Deviation (grams)
0	927	44
96	920	40
249	878	70
509	793	19

Figure 24. Pull strength decreases with isothermal aging at 125°C for 509 hours for the 1517 I/O LGA with columns.

Optical photomicrographs of solder joints and columns after exposure at 125°C for 509 hours are shown in Figure 25. Many pockets within the fully populated columns were randomly selected to perform pull testing at various intervals. Shown are failures of columns and copper spiral, as well as micro-structural changes due to isothermal aging at high temperature. Failures under all conditions—as built and isothermal aging to 509 hours—were from columns rather than within solder or at the interface between solder and pad.

Figure 25. Failure and microstructural changes after 509-hour isothermal aging at 125°C.

5.3 Attachment Procedures

Initial assembly focused on optimization of paste print and reflow for the columned LGA packages, even though a large number of fine pitch array advanced packages and leaded quad flat packages were designed close to the CGA packages. After paste prints and inspection characterization to assure their acceptance, then, CGAs were placed onto solder paste using a rework station.

Solder paste areas and heights were measured using a laser interferometer profilometer with sophisticated three-dimensional (3D) measurement capability. Measurements were made at numerous locations—including corner and center pads—to gather solder volume data and their corresponding distributions.

Figure 26 shows representative examples of photomicrographs of CGA1517 pads after solder paste deposition and their characteristic parameters, including height values for type V

paste. These figures also show color-coded height distribution of solder paste print for these set of pads. Overall, no major manufacturing issues were found with the paste depositions for the columned LGA with 1.0-mm pitches. Type IV paste print quality was similar, so it is not reported.

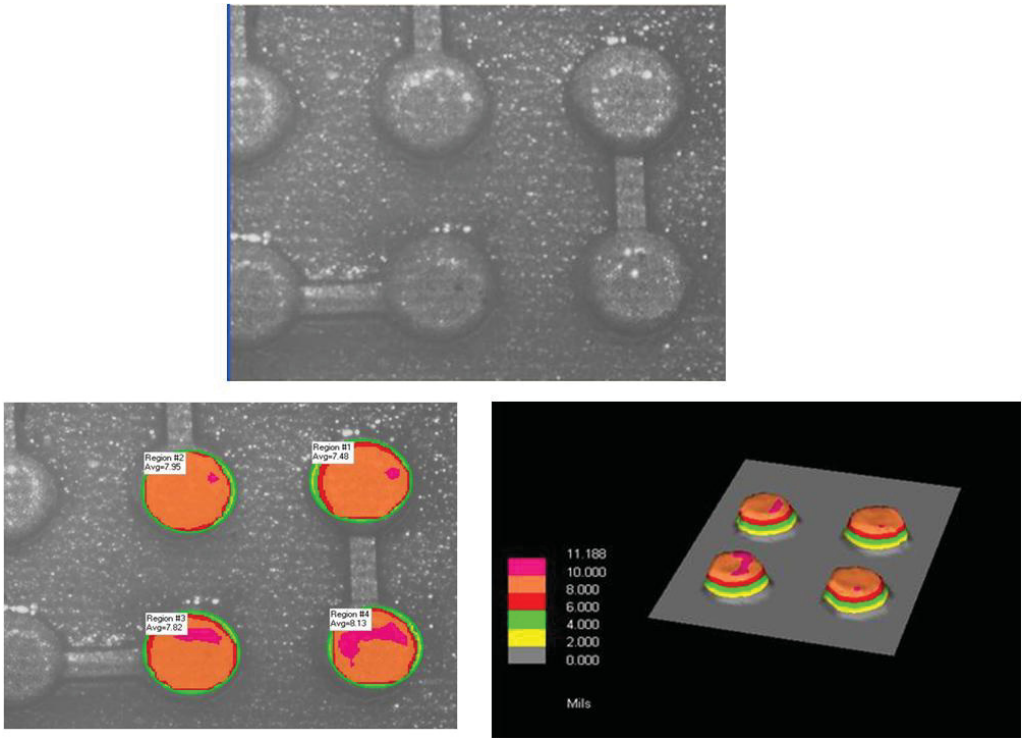


Figure 26. Type V solder paste print quality and color-coded height distribution for CGA1517 I/O.

Solder paste reflow was performed using a vapor phase reflow machine set up for tin-lead process. Reflow profiles were tailored based on a previously established profile, the same profile as narrowed for other CGAs.

5.4 Optical Microscopy Characterization of LGA/CGA

5.4.1 After Assembly

LGAs with copper spiral solder columns and those with micro-springs coils were assembled onto two different PCBs with both standard and lower pad diameters; this accommodated the two column/spring diameters. During the processing of LGAs with micro-spring coils, a CGA1272 was also assembled onto the board as a baseline for process and reliability evaluation. Visual inspection of peripheral columns was performed for these assemblies since the board was designed for visual characterization, especially since most of the PCBs were only populated with CGAs. Only outer rows, and in some cases, second and third rows, could be assessed for solder joint quality. Verification by daisy chain resistance measurement was not possible since LGAs had no daisy chain package design. The photomicrographs in Figures 27 and 28 show the quality of solder joints for micro-spring coil column CGA assemblies. Note that solder joint fillet

formations are different since there are no solid solder columns; however, good quality solder fillet formation is apparent.

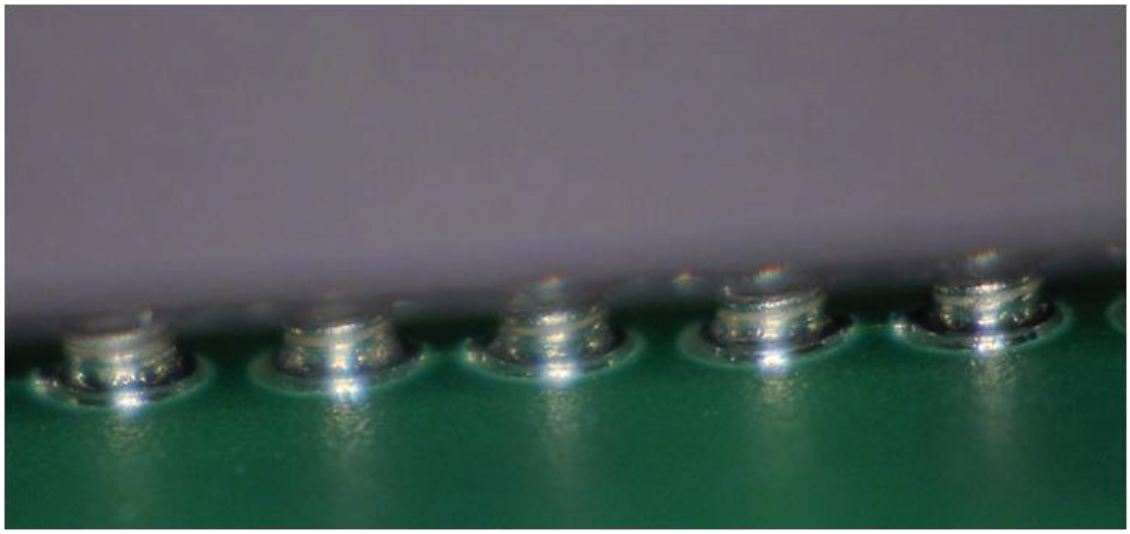


Figure 27. Representative photomicrographs of solder joint quality after assembly for micro-spring coil column CGA1571.

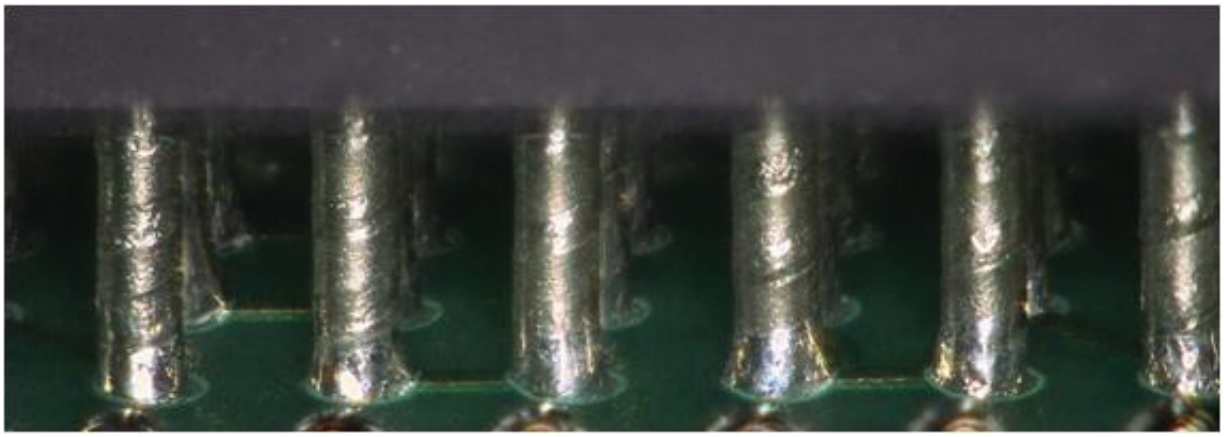


Figure 28. Representative photomicrographs of solder joints quality after assembly for CGA1571 with copper-wrapped solder columns.

6. Interim Results

This interim report presented preliminary test data for CGA packages with 1752 and 1272 inputs/outputs (I/Os) and 1-mm pitch. It presented visual, SEM, and thermal cycle reliability evaluation performed on a CGA1752 package to determine the integrity of a large number of chip capacitors that are surface-mounted onto the CGA ceramic substrate. Analysis showed that these capacitors are assembled with a high-lead tin-lead solder alloy that did not melt during column attachment using a lower melting temperature of eutectic tin-lead solder, and will not reflow during package assembly operations using the same alloy composition. No failures of the high-lead solder joints were observed when a package was subjected to 200 thermal shock cycling in the range of –55° to 130°C, with 10 minutes dwell times at the two extreme temperatures.

These large packages with two different column styles (pure-solder and copper-wrapped columns) were assembled onto conventional printed circuit boards using standard tin-lead solder paste alloys. Inspection was performed to determine the quality and volume of solder paste print for three solder paste types. The inspection results were presented for the solder paste prints, as well as those performed later for assembly solder joints. The quality of solder joints was considered to be acceptable based on visual inspection of peripheral solder joints. X-ray photomicrographs showing the quality of solder joint assemblies and workmanship defects revealed no shorts or significant solder balling.

The investigation also included a ceramic array package with 1517 I/Os that originally was a land grid array (LGA) package. A number of LGAs were converted to CGAs by performing column attachment using two different column styles. For one column style, the integrity of column attachment was established by subjecting columns to pull testing, first as attached and, subsequently, at intervals during isothermal aging at 125°C. The pull test results to 500 hours of aging showed some signs of column degradation, but no change in failure mechanism. All failures were due to column/copper wrap failures with no solder failures at column/package interface.

The test plan matrix clearly documented key variables for advanced and extremely large ceramic area array packages, both LGA and CGA package styles. It was demonstrated that LGAs can be converted to CGA packages using different column types-solder columns with copper wrapping or micro-spring coils with no solder columns. It also was shown that the CGA versions of LGA packages can be assembled onto PCB if the PCB pad design and other processing parameters are appropriately optimized for the type/size of package and column. Extremely large/thick CGA packages with 1752 I/O were successfully assembled onto PCBs. Reliability is a key issue that was addressed for the chip capacitors on packages, but the overall assembly reliability is currently being evaluated and will be included in the final report for both conventional and HDI PCBs.

7. Acronyms and Abbreviations

BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
COTS	commercial-off-the-shelf
CQFP	ceramic quad flat pack
CSP	chip scale (size) package
CTE	coefficient of thermal expansion
Cu	copper
DOE	design of experiment
EDX/EDS	energy dispersive x-ray
FPGA	field programmable gate array
FCBGA	flip-chip ball grid array
HASL	hot-air solder leveling
HDI	high density interconnect
I/O	input/output
JPL	Jet Propulsion Laboratory
LGA	land grid array
MIP	mandatory inspection point
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
NSMD	non solder mask defined
PBGA	plastic ball grid array
PCB	printed circuit board
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
RMA	rosin mildly activated
SEM	scanning electron microscopy
SMC	surface mount components
SMD	solder mask defined
SMT	surface mount
Tg	glass transition temperature
TV	test vehicle

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14. ABSTRACT

This interim report presents test data for CGA packages with 1752 and 1272 I/Os and 1-mm pitch. It includes the results of visual, SEM, and thermal cycle evaluations performed on the CGA1752 packages to determine the integrity of the chip capacitors on package. After integrity was established, packages were assembled onto conventional printed circuit boards using standard tin-lead solder paste alloys. Inspection was performed to determine both the quality of solder paste prints and the volume of three solder paste types with different solder particulate sizes. Results are also presented for inspections performed on two packages with different dimensions and column types. X-ray photomicrographs show the quality of solder joint assembly and workmanship defects. Evaluation also included a ceramic array package with 1517 I/Os that was originally an LGA. A number of LGAs were transformed into CGA by performing column attachment using two different column styles. The integrity of column attachment for these was established by subjecting them to pull testing; first, as attached and, subsequently, at intervals during isothermal aging at 125°C. The pull test results are shown.

15. SUBJECT TERMS
CGA, CCGA, Solder joint reliability,thermal cycle, column grid array, 2nd level reliability

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